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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,446	01/20/2004	Daniel Frank Moertl	ROC920030380US1	9233

30206 7590 12/12/2005

IBM CORPORATION
ROCHESTER IP LAW DEPT. 917
3605 HIGHWAY 52 NORTH
ROCHESTER, MN 55901-7829

EXAMINER	
SUN, SCOTT C	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 12/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,446	MOERTL ET AL.	
	Examiner	Art Unit	
	Scott Sun	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413). Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 1-23 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for a second clock frequency (read clock) or (exclusive) data width being selectively provided for outputting data and control information from a FIFO RAM with no back pressure, it does not reasonably provide enablement for a first clock frequency (write clock) and a second clock frequency (read clock) and data width being selectively provided. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. Specifically, the specification explicitly states two options: adjusting the B-SIDE (read) clock frequency; and adjusting the width of the FIFO RAM (page 6, lines 8-13) which are clearly presented as exclusive choice of one or the other, since each option accomplishes the function independently from the other. In addition, the specification also does not disclose adjusting write clock frequency as an option for eliminating back pressure. The examiner suggest that the claim language be changed to reflect the actual device/method presented in the specification or the specification be amended to enable a person of ordinary skill in the art to make and use the invention as claimed. For example, lines 11-14 of claim 1 can be changed to "either said second clock frequency

or a data width of said FIFO RAM being selectively provided for outputting said data and control information from said FIFO RAM with no back pressure". For the purpose of continuing prosecution, the examiner will interpret the limitation as the previous example.

3. The following rejections are made based on the examiner's best interpretation of the claims in light of the 35 USC 112 rejections above.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 6-9, 11, 13-18, 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (PG Pub US 2003/0177295) in view of Aipperspach et al. (PG Pub #US2003/0128611).

6. Regarding claim 1, Hsu discloses a flow through asynchronous elastic first-in, first-out apparatus (system in figure 5) comprising: a FIFO RAM having a data input (input port in paragraph 24) for receiving data and control information and a data output (output port in paragraph 24) for outputting said data and control information (column 3, lines 10-15); said FIFO RAM including a plurality of locations for storing a plurality of words, each word including a set number of bits; The examiner asserts that a person of ordinary skill in the art would readily recognize that a FIFO can store both data and

control information, such as packet headers. A person of ordinary skill in the art would further recognize that memory are designed to have memory cells (bits) that form a plurality of words.

Hsu further discloses a write clocked logic (Wptr in figure 5, paragraph 24) for loading said data and control information to said FIFO RAM at a first clock frequency. Asynchronous read clocked logic (Rptr in figure 5, paragraph 24) for outputting said data and control information from said FIFO RAM at a second clock frequency. The examiner asserts that by definition of asynchronous FIFOs the read and write frequencies are asynchronous to each other.

Hsu does not disclose explicitly selectively providing first frequency, second frequency, and a data width. However, Aipperspach discloses a data width of a FIFO RAM being selectively provided for outputting data and control information from said FIFO RAM with no back pressure (system in figure 2; paragraph 16, 20). The examiner asserts that Aipperspach discloses the system for adjusting for discrepancies between write and read frequencies, which is the cause of back pressure as disclosed by the applicant (when writes are faster than reads). Therefore Aipperspach's system also accomplishes the intended use as disclosed by the applicant. Furthermore, the examiner refers the applicant to the above 112 rejection for examiner's interpretation of the limitation.

Teachings of Hsu and Aipperspach are from the same field of asynchronous FIFOs. Therefore, it would have been obvious to a person of ordinary skill at the time of invention to combine Aipperspach's and Hsu's teachings by implementing the multi-

mode technique disclosed by Aipperspach in the system disclosed by Hsu to enable the FIFO RAM to operate at two or more different data widths for the benefit of connecting the FIFO to multiple devices operating at different frequencies to reduce memory occupancies (Aipperspach, paragraph 7)

7. Regarding claim 2, Hsu and Aipperspach combined disclose claim 1, and Aipperspach further discloses wherein said FIFO RAM includes a multiple location FIFO RAM used on each asynchronous boundary (paragraph 15). The examiner asserts that Aipperspach discloses the FIFO interfaces between different applications operating at different frequencies, which are asynchronous boundaries.

8. Regarding claim 11, Hsu and Aipperspach combined disclose claim 1, and Hsu further discloses wherein said write clocked logic for loading said data and control information to said FIFO RAM at said first clock frequency includes a Gray code increment block encoding a write address input to said FIFO RAM (Wmaster in figure 4, paragraph 24).

9. Regarding claim 13, Hsu and Aipperspach combined disclose claim 12, and Hsu further discloses a pair of synchronization latches to provide a synchronization input to said asynchronous read clocked logic for outputting said data and control information from said FIFO RAM at said second clock frequency (synchronization circuits in figure 6, paragraph 24). The examiner notes that Hsu discloses the sync circuits can be flip-flops (which are latches).

10. Regarding claim 14 and 15, the examiner asserts that Hsu further discloses the write and read Gray code circuits are identical (last line of paragraph 2). Therefore the same arguments used in rejection of claims 11 and 12 are used.

11. Regarding claims 6-9, Hsu and Aipperspach combined disclose claim 1 but do not disclose explicitly using data and control field to select and write data to a target engine. However, the examiner asserts that a person of ordinary skill in the art at the time of invention would readily recognize that data transferred have control information (for example the header of a packet) indicating the destination, including engine and buffer, of the data.

12. Regarding claims 16-18, 20-22, the examiner asserts that these claims are substantially similar to claims 1, 6-9. Specifically, claim 16 and 17 are similar to claim 1, claim 18 is similar to claim 8, claim 20 is similar to claim 6, claim 21 is similar to claim 7, and claim 22 is similar to claim 9. They are rejected using the same arguments.

13. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (PG Pub US 2003/0177295) in view of Aipperspach et al. (PG Pub #US2003/0128611) and further in view of Adamchick (US Patent #4,122,520).

Hsu and Aipperspach combined disclose claim 1 but do not disclose explicitly using DMA. However, Adamchick discloses using a DMA system (figure 3a). It would have been obvious for a person of ordinary skill in the art at the time of invention to combine Adamchick's teachings with teachings of Hsu and Aipperspach by using DMA, as disclosed by Adamchick, to direct data transfer through the FIFO RAM system

disclosed by the combined teachings Hsu and Aipperspach for the benefit of altering the contents of a memory without altering the speed of CPU (column 1, lines 6-10). The examiner further asserts that the use of DMA to direct data transfer has been well known for many forms of data transfer in general, and that a person of ordinary skill in the art would readily recognize that DMA can be used to direct data transfer through a FIFO RAM as well.

14. Claim 5, 10, 19, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (PG Pub US 2003/0177295) in view of Aipperspach et al. (PG Pub #US2003/0128611) and further in view of Lee (PG Pub #US 2004/0093443).

15. Regarding claim 5, Hsu and Aipperspach combined disclose claim 1 but do not disclose explicitly using ECC. However, Lee discloses using ECC in a FIFO system (figure 8). Therefore, it would have been obvious to combine Lee's teachings with teachings of Hsu and Aipperspach by adding ECC checking step disclosed by Lee in the combined system of Hsu and Aipperspach for the benefit of detecting and correction errors during data transfer.

16. Regarding claim 10, Hsu and Aipperspach combined disclose claim 1 but do not disclose explicitly using control field to authorize for discarding data. However, the examiner asserts that a person of ordinary skill in the art at the time of invention would readily recognize that data no longer needed such as data containing errors are discarded. For example, Lee teaches that data in a FIFO is discarded (deleted) after an error is found (figure 8). The examiner further asserts that a person of ordinary skill in

the art would readily recognize that some type of data (for example, 1 bit in the header of data packet) is used to mark (authorize) a packet of data for discarding.

17. Regarding claims 19 and 23, the examiner asserts that these claims are substantially similar to claims 5 and 10. Specifically, claim 19 is similar to claim 10 and claim 23 is similar to claim 5. They are rejected using the same arguments.

18. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (PG Pub US 2003/0177295) in view of Aipperspach et al. (PG Pub #US2003/0128611) and further in view of Lowe et al (US Patent #6,937,172).

19. Hsu and Aipperspach combined disclose claim 11 discloses Gray code increment block but do not disclose explicitly a multiplexer coupled to said Gray code increment block. However, Lowe discloses a multiplexer coupled to a Gray code increment block (figure 9D) and receiving a write strobe select input (step 998, pointer increment assertion) for incrementing a Gray code write address (step 997). Lowe's teachings and teachings of Hsu and Aipperspach are from analogous art of FIFOs (see Lowe's background section).

Therefore, it would have been obvious at the time of invention to combine Lowe's teachings with combined teachings of Hsu and Aipperspach by adding the multiplexers disclosed by Lowe into the combined system of Hsu and Aipperspach for the benefit of selecting a between incremented value and a register value (column 13, lines 43-48).

Conclusion

20. Other publications are cited to further show the state of the art with respect to FIFO architechture. Refer to form 892, "Notice of References Cited", for a complete list of relevant prior arts cited by the examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Sun whose telephone number is (571) 272-2675. The examiner can normally be reached on M-F, 10:30am-7pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS – 12/2/2005

KIM HUYNH
PRIMARY EXAMINER
12/7/05